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Investigation on Geometrical Effects of FinFET Electronic Device Properties Using TCAD Simulations and Taguchi Optimization

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ABSTRACT

To ensure optimal operating conditions and performance, transistor dimension parameters must be determined accurately. This work investigates the Taguchi approach for device parameter optimization in a 7nm Silicon FinFET, employing design of experiments (DOE) methodologies to improve device performance and efficiency. In this work, the geometric scaling that affect FinFET performance, with an emphasis on the ratio of on-state current (ION) over off-state current (IOFF), threshold voltage (VTH), subthreshold swing (SS) and drain induced barrier lowering (DIBL) are investigated. The Taguchi approach is used to optimize the FinFET model, resulting in improved performance. Furthermore, investigation on the impact of optimized FinFETs on logic circuit performance, notably delay and power characteristics. Moreover, the Silvaco TCAD Simulator is used as the medium of simulation and analysis. The Taguchi method was implemented to determine the most appropriate combination of factors for robust device performance using orthogonal arrays, and signal-to-noise (SN) ratio as the quality characteristic of choices. The factors involved in the design of experiments include the length (LG) and height (HFIN) of the fin as well as the width (WFIN) of the fin at the top region. Using Taguchi's robust performance signal-to-noise ratio, the combination of parameters was obtained for the ION/IOFF ratio, VTH, DIBL, and SS. The VTH value is 0.7461V for FinFET with LG, WFIN, HFIN being 13 nm, 7 nm, and 35 nm, respectively. The current ratio of 262.072 and SS of 69.4 mV/dec obtained from FinFET when LG is 13 nm, WFIN is 5 nm, and HFIN is 40 nm. For the optimum DIBL, which is 232 mV/V, is gained when the FinFET has LG, WFIN, and HFIN 10 nm, 10 nm, and 35 nm, respectively. The analysis confirms that dimension optimization can significantly enhance FinFET performance. The use of the Taguchi method proved effective in identifying the optimal parameter combinations, and the subsequent application to logic circuits for the development of low-power FinFETs.

Keywords: *design of experiments (DoE), SiO2, off-current (IOFF), on-current (ION), SN ratio, Taguchi method, TCAD simulation, fin length (LG), fin height (HFIN), fin width (WFIN) threshold voltage (VTH), subthreshold swing (SS), drain induced barrier lowering (DIBL)*

1. INTRODUCTION

FinFET is a potential successor for CMOS device architectures in the nanometer range. It provides great control over SCEs (short channel effects) such as leakage current, DIBL, and perfect sub-threshold slope. Because 7nm FinFETs have less critical dimensions, they contribute to improved performance by providing significant channel control. According to ITRS, FinFET will propel technology from the sub-nanometer range up to the 5nm node. [1], [2]. Various manufacturers, including Samsung, Global Foundry, and Intel, are working at the 14 nm node. Broadwell-y, an Intel Core M processor, is built on 14nm technology. Intel is primarily focused on optimizing FinFETs by increasing HFIN. FinFET VTH properties are determined by HFIN and WFIN. In this work, the design optimization of FinFET performance is focusing on device dimension consisting of channel length, finger width and finger height. The electrical characteristics of a 7nm FinFET includes VTH, ION/IOFF ratio, SS, and DIBL are optimized using the Taguchi method and design of experiments. To understand the performances characteristics, the effects of varying fin LG, WFIN, and HFIN on VTH, ION/IOFF ratio, SS, and DIBL are studied

2. LITERATURE REVIEW

The short channel effect occurs when the conductive channel length of a FinFET is less than 20 nanometers, or even ten nanometers. The impacts of decreasing channel length include lower threshold voltage, and lower leakage-induced barrier. Shorter gate lengths in FinFETs lead to less channel control capacity. This makes it difficult for the gate voltage to push off the channel, resulting in sub-threshold leaking. The short channel impact is more likely to occur [3]. Generally, LG should be more than or equal to Fin Width for better DIBL control and a current ratio. DIBL is a unique method for assessing short-channel effects in electronics. DIBL tends to increase when LG scales down, with its LG being determined by the scaling length of the devices. [4]. The FinFET structure was created to address MOSFET scaling issues, which limited devices scalability. High

leakage current in short channel transistors reduces switching performance by lowering the ION/IOFF ratio. ION and IOFF are key electrical characteristics used to evaluate device performance, especially switching speed and standby time [5]. To obtain reliable switching performance, Ion should be higher and IOFF as close to zero as possible, resulting in a high ION/IOFF ratio. Off-state leakage current is also reduced by technology. However, the older MOSFETs have surpassed their key scalability and performance limits. One major downside of this device is its extremely low threshold potential, which allows for quick device startup [6] [7]. The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage [8]. In FinFETs, the VTH can be reduced to improve device performance while also reducing leakage current significantly [9]. The SS increases significantly when the gate length is shortened. The SS increases when the drain-to-source voltage increases. It is caused by the enhancement of subthreshold current due to lowering the potential barrier height by drain effect. [10] Conclude that it aims to optimize the electrical characteristics of a 7nm FinFET using the Taguchi method and design of experiments. Moreover, it investigates the effects of varying fin LG, WFIN, and HFIN on VTH, ION/IOFF ratio, SS, and DIBL.

3. METHODOLOGY

Figure 1 shows the flowchart to represent project's technique. First, it will design the FinFET technology behaves based on its factors that will be used. To progress technology, this involves evaluating the device's attributes, capabilities, performance, and other areas. The TCAD simulation will optimize and make use of all the study data that has been gathered. We will assess the performance and examine the effects of lowering the geometric and parametric parameters of the FinFET based on the results of the simulation. With the aid of this data, the settings that provide the device with its best performance characteristics can be found

3.1. Silvaco TCAD

The research was carried out using simulation in the SILVACO TCAD software. The source and drain lengths (LS/LD) and gate lengths (LG) in nanometers are the parameters utilized in the FinFETs. WFin is the width and HFin is the height of the vertical silicon fin. The source and drain areas are doped with 1.20×10 cm^{-3} donor concentration, whereas the channel is evenly doped with 1.45×10 cm^{-3} acceptor dopant. Figure 1 shows the flowchart of Silvaco TCAD simulation. Figure 2 shows the 3D structure of the FinFETs used in this work. The simulation used 2D Schrodinger-Poisson model, and the quantization inside the channel is nearly 2-dimensional. Equation 1 and 2 are used in the simulation to extract subthreshold swing and the DIBL respectively [5].

$$SS = \frac{dV_{GS}}{d(log_{10}I_{DS})} \quad (1)$$

$$DIBL = \frac{\Delta V_{TH}}{\Delta V_{DS}} \quad (2)$$

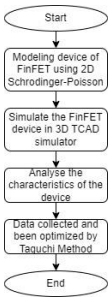

Figure 1. Flowchart of Silvaco TCAD simulation

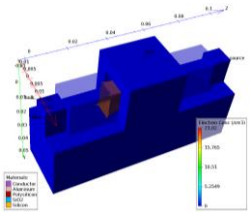

Figure 2. 3D structure of the FinFETs from the SILVACO TCAD Simulation.

3.2. Taguchi Method

The Taguchi method is one of several statistical strategies that are highly beneficial to answer complex and difficult problems with the fewest variables and fewer tests in numerous domains [11]. The Taguchi approach aims to find the parameters or factors that have a substantial impact on product performance. Hence, it employs orthogonal arrays to systematically vary simulation parameters and analyze their influence on target performance metrics. In this study, the Taguchi method was used to optimize the FinFET device geometry by exploring the impact of three key factors such as channel length (Lg), fin width (Wfin), and fin height (Hfin) on threshold voltage (Vth), Ion/Ioff ratio, subthreshold swing (SS), and drain-induced barrier lowering (DIBL).

To study the effects of each parameter variation. Table 1 summarizes the three-level design of experiments, with each factor assigned levels 0, 1, and 2. The L27 orthogonal array (3^3 design) was selected to balance design comprehensiveness with computational efficiency. Each simulation scenario corresponds to one combination of parameter levels [12].

Table 1. Factors and levels used in the parameters

Symbol	Factors	Level		
		0	1	2
A	Channel Length	10	13	15
B	Fin Width	5	7	10
C	Fin Height	30	35	40

Parameters that have been varied are shown in Table 1 which are LG, WFIN, and HFIN which were assigned as A, B and C respectively. These factors are set at three levels each, where '0' defines the least value while '2' defines the biggest. Meanwhile, the responses or the desired output measures are the VTH, ION/IOFF, SS, and DIBL using the smaller the better (STB), the larger the better (LTB) and the nominal the better (NTB) respectively.

The three-level standard orthogonal arrays used in this work is L27(33) [12]. In this work, the factors level is varied by previous work, where it researches to optimize the FinFET [13] [14]. In addition, all the design parameters and electrical characteristics of the structure were calibrated as per the guidelines of ITRS.

3.3. Synopsis Hspice

FinFET library from Predictive Technology Models (PTM) is used in this work. These predictive files were chosen because they are compatible with the HSpice simulator and can handle a wide range of process changes. Following that, a simulation will be run using data from the Taguchi method, with the primary goal of optimizing both delay and power consumption in the circuit. Inverter circuits are used in this work to study delay and power consumption. Figure 3 shows the flowchart of simulation on Hspice.

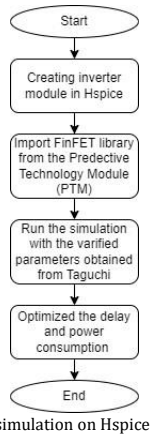

Figure 3. Flowchart of simulation on Hspice

4. RESULTS AND DISCUSSION

In this section, the effect of variation in WFIN, LG, and HFIN on the electrical characteristics of devices has been discussed. The objective of this paper is to optimize VTH, ION/IOFF, SS, and DIBL use the DOE based on the WFIN, LG, and HFIN. The VTH, ION/IOFF, SS, and DIBL performances of the FinFET statistically using the Taguchi method. Should the device aim for higher ION/IOFF ratio, the LTB characteristic is applied to perform the DOE. In terms of IOFF performance, the device requires low subthreshold leakage thus using the STB characteristics. Meanwhile in terms of VTH, the LTB characteristic is applied to perform the experiments.

4.1. Effects of physical parameters variation on V_{TH}, I_{ON}/I_{OFF} RATIO, SS and DIBL

For FinFET devices, the threshold voltages may be adjusted by imposing the various gate materials, whose work function may play crucial roles in controlling the values of threshold voltages. The VTH is nominal at all points, which makes all the parameters combination does not make too much difference. The threshold voltage (Vth) was extracted using the constant current method, defined as the gate voltage (Vg) at which the drain current (Id) reaches 10^-7 A/μm, under a drain bias of Vds = 0.7 V. This method ensures consistent comparison across device geometries.

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The proposed 7nm device has a higher ION/IOFF ratio that is satisfactory for any electrical device [15]. Having higher HFIN can give a higher ION/IOFF ratio. Hence in terms of ION/IOFF ratio proposed device have higher value, so it performs much better from the older MOSFET. From the existing technology it is found that the proposed 7nm device operates with minimal leakage and drive current along with a better ION/IOFF ratio. Furthermore, when it indicates that as the channel length is decreased, the SS can be the better immunity to SCEs. Figure 4(C) shows the subthreshold swing roll-up versus the channel length for different fin width. In comparison, the smaller width is 5nm, the more subthreshold swing can roll-up. The main reason is that the width can induce a shorter scaling length, which hence results in less subthreshold behavior degradation than the wider one [16]. As the LG is narrowed down to 10nm, the DIBL effect is more distinct. However, the trend of DIBL in short-channel devices with channel widths is clearly increased, but not consistent. This phenomenon is perhaps that the etch bias is not easily controlled. As the channel width is increased, the DIBL is increased due to the better uniformity of threshold voltage implantation. When the channel length is increased, the DIBL value is also increased. The cause is like the statement at the DIBL discussion. The internal electrical filed due to the LG brings down the impact of punch-through effect [17].

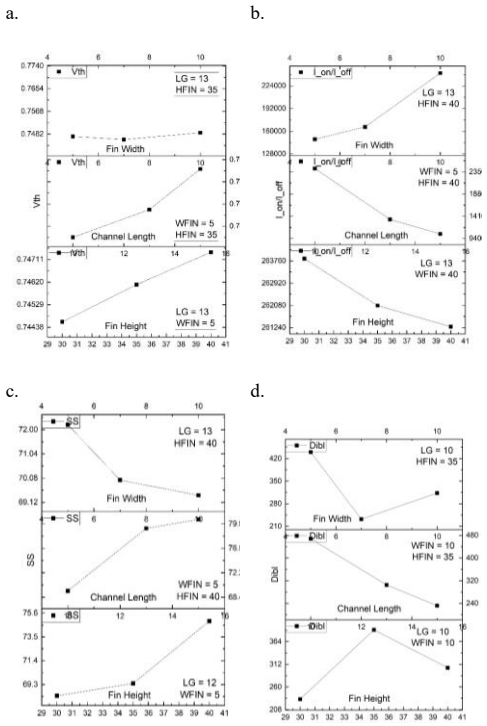

Figure 4. Effect of a) VTH, b) ION/IOFF, c) SS, and d) DIBL on different L_G, W_{FIN}, H_{FIN}

4.2. Optimization of VTH, ION/IOFF RATIO, SS and DIBL.

The effects of geometry scaling resulting in VTH are presented in figure 4(a), with the optimization VTH is getting smaller. The combination of geometry shows that LG is 13nm, WFIN is 7nm, and HFIN is 35nm. The VTH is 0.7461V did cause of the source-drain regions are very close with each other to the point that the current charge being controlled by gate is reduced. Some of the charges allow flow between the source and the drain in the channel, hence lowering the VTH. However, further reduction of the parameter shown decreasing unstable of device and probably implying that SCEs is getting worse. Moreover, figure 4(b) shows the SNR of the three factors on ION/IOFF characteristics. As the device shrinks, the ION/IOFF shows huge improvements with the combination that gained from the Taguchi, the ratios mostly up to 106. The combination to get the optimum ratio are LG is 13nm, WFIN is 5nm, and HFIN is 40nm. The rising ION/IOFF drops drastically at Lg around 15 nm indicating the relative increase in IOFF is substantial compared to the small increase of ION. This observation is essential since it demonstrates how the combinations parameter can affect the performance of FinFET. The effect of reducing parameters has given the output of higher ratio of ION/IOFF. When the ratio increases, it shows that the device is becoming faster and reducing the leakage current. The figure and table below show the effect of each factor that relates to the current ratio. It represents the optimize combination based on the SNR. Then, from figure 4(c), it can be observed that the SS is better when the parameters LG is 13nm, WFIN is 5nm, and HFIN is 40nm. It gives the SS result as 69.4mV/dec which happens to give low power, because of lower SS reduce the power. Fundamentally reducing the voltage to achieve desired on-off switch [18]. The obtained of SS in this analysis provides a rough qualitative sign of the reducing of short channel effect (SCE) of a short transistor. Lastly, as shown in figure 4(d) DIBL results in lowering of barrier height of a the FinFET due to drain voltage. DIBL must be less so that device can go to off condition. The higher the value, the more chance a device failed to go in off condition. DIBL on FinFET depends on Fin width. The channel length must be greater or be the same as Fin width to effectively suppress DIBL [19]. Based on the result it shows that the combination of parameters LG is 10nm, WFIN is 10nm, and HFIN is 35nm have given the effective DIBL which is around 232 mV/V.

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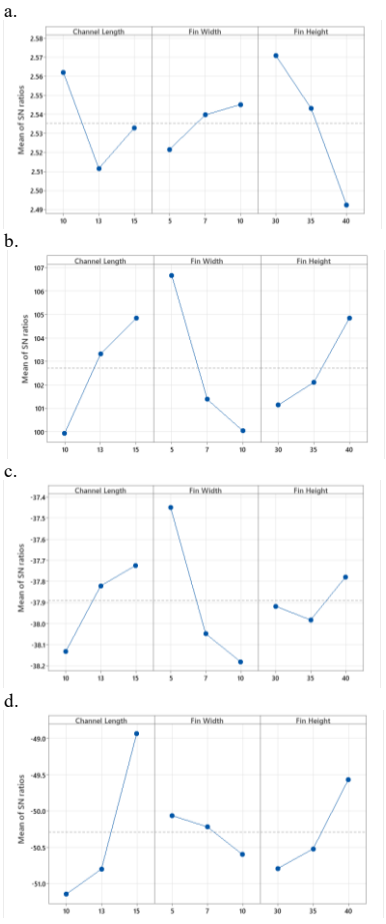

Figure 5. average SNR against factor level for a)VTH b)ION/IOFF c)SS d)DIBL on channel length, fin width and fin height.

4.3. Pareto Analysis of Variance (ANOVA)

To validate the results, the contribution of each geometrical parameter to each device's performance was further investigated by applying ANOVA. Figure 6 the Pareto diagram of designs aiming

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for an efficient VTH, ION/IOFF, SS, and DIBL performances, for the FinFET, respectively. It is observed that interaction for all parameters, in all characteristics. The interaction is classified as (A×B), (A×C), and (B×C). The NTB analysis was chosen for the optimal VTH, which is justified. Following the next characteristic, which is the current ratio, the interaction demonstrates that the LTB analysis produced the same result as Taguchi. Furthermore, the SS and DIBL determined by LTB analysis have been supported by the interaction depicted in the figure 5(a) and 5(d). Following the result gain, it approves that every combination gives the optimum result between the interactions.

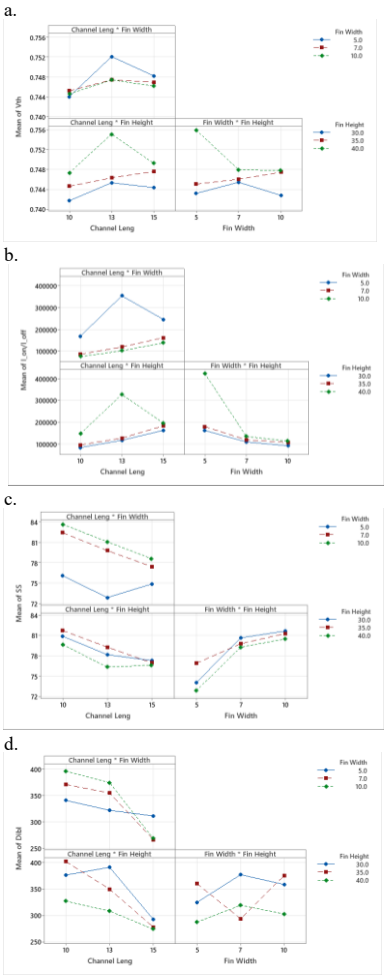

Figure 6. Average SNR against factor level for a) VTH b) ION/IOFF c) SS d) DIBL on channel length, fin width and fin height.

4.4. Implementation on inverter performance for circuit level optimization.

Table 2 demonstrates that the power of this work is improved with this combination parameter at the nanoscale as compared to others. The VTH optimization 33 combinations achieved a 46.9% improvement in faster delays and a 93.8% reduction in power consumption compared to the default configuration. These improvements are due to the low voltage used to reduce power consumption. It has been established that the smaller the device, the lower the voltage that can be employed for low-power applications. The delay can be compared between the default settings, and it is observed that the delay is improved in this work.

Table 2. Power and delay for each optimization combination.

Type	Delay	Power
This Work	1.01E-08	6.13E-12
Default	1.900E-08	9.833E-11
Paper 1[20]	-	3.989E-9
Paper 2[21]	-	2.807383E-9

5. CONCLUSION

In this study, the influence of geometric scaling and process parameters on the performance of FinFETs, with a specific focus on key performance indicators such VTH, current ratio, SS and DIBL. FinFET performance is considerably improved by lowering geometric dimensions and optimizing process parameters, especially for low-power applications. The findings demonstrate a significant reduction in SCE and a significant improvement in on-current while maintaining a low off-current. The VTH, SS, and DIBL measurements also show improved device stability and performance, confirming the efficiency of these parameter changes for achieving low-power, high-performance FinFETs. The Taguchi approach was then used to optimize the FinFET model, with the goal of increasing the current ratio and improving transistor performance while reducing leakage current. With the Taguchi approach, the design space was effectively explored, and an ideal set of parameters was developed. The SNR analysis revealed that the chosen parameter combination is the most effective at meeting the intended performance targets. This optimization procedure not only improved overall performance metrics but also validated the resilience and reliability of the Taguchi method in semiconductor device optimization. Using the optimized FinFET characteristics in a logic circuit, especially an inverter circuit in HSPICE, resulted in considerable gains in circuit performance. The optimized inverter demonstrated lower power consumption and smaller delay, making it ideal for low-power applications.

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