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Electrical Performance Evaluation Based on Design Parameters of Silicon Nanowire Gate-All-Around (GAA) TFET

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ABSTRACT

The SiNW GAA is one of the technologies with potential for better short channel behavior and gate control over conductivity. This work investigates the effect of various geometrical dimensions of Silicon Nanowire Gate-All-Around Tunneling Field Effect Transistor (SiNW GAA TFET) on electrical characteristics. The design parameters consist of gate oxide thickness (T_{OX}), channel radius, dielectric material, gate metal work function and low/high drain voltage are varied in the simulation process to analyze the electrical performance of SiNW GAA TFET. Subthreshold Slope (SS), I_{ON}/I_{OFF} current ratio and threshold voltage (V_{th}) are extracted. The result shows that the oxide thickness of 3 nm, the channel radius of 10 nm - 18 nm and SiO_2 as a dielectric material tend to have the best SiNW GAA TFET characteristics. While the work function of gate metal TiN and drain voltage of 0.5V are the most effective for the device performance. This study highlights the potential of GAA nanowire TFETs to drive innovation in semiconductor technology through superior electrical performance.

Keywords: *SiNW GAA TFET; gate oxide thickness TOX; channel radius; dielectric material; gate metal work function; drain voltage; Subthreshold Slope (SS); I_{ON}/I_{OFF} current ratio; Threshold Voltage (V_{th})*

1. INTRODUCTION

The scaling of metal-oxide-semiconductor field-effect transistor (MOSFET) has continued since the development of integrated circuits in the 1950s, with the emergence of new technologies to extend complementary metal-oxide-semiconductors (CMOS) down to ever lower technological nodes. However, because of basic physical and technical restrictions, CMOS scaling has varied from Moore's predicted trends and Dennard scaling's principles [1]. Moore's Law states that for every 24 months, the number of transistors on a chip doubles its number [2]. This law caused every company involved in semiconductor and microelectronic industry to compete with each other to achieve a better performance device and meet every demand in present society.

Heat dissipation, leakage current, and channel length modulation have all become serious concerns, which will eventually slow down CMOS scaling as we get closer to the atomic dimension. As a result, new semiconductor technology is urgently needed to address challenges like cost, speed, reliability, and power dissipation. There has been a lot of effort put in, among all the candidates, Nano-electronics involving the replacement of existing silicon-based technology has emerged as one of the most promising solutions for continuous CMOS scaling [1].

In recent decades, bottom-up semiconductor nanowires and derived field-effect transistor (FET) devices have been extensively explored as the essential building blocks for nano electronic devices and circuit technologies. Nanowires have a smaller channel and a higher surface-to-volume ratio than planar devices made of bulk materials. Furthermore, the gate surrounding or gate all around (GAA) structure that may be produced in nanowire FETs provides good electrostatic gate control over the nanowire channel.

Silicon Nanowire FET were listed as one of the most promising emerging logic devices, but the device features and configuration have a limited reliability and detailed research on the reliability of SiNWT is uncommon [3]. With the size reduction of Si-based field-effect transistors (FETs), the reliability and performance of these Si-based MOSFETs are a bit worrying. In addition to their limitations in fabrication and scaling for threshold voltages, gate oxide thicknesses, leakage currents, the occurrence of short channel effects (SCEs) such as subthreshold slope (SS) and gate current leakage in the transistor make the scaling process complicated.

Meanwhile, on the further study to overcome the problems, the Cylindrical Gate all around (GAA) MOSFET is considered as the device with potential for CMOS technology. Studies in [4], [5] specify that the GAA FET

exhibit superior performance rather than other devices in terms of scaling of SCEs such as subthreshold slope (SS), threshold voltages (Vth) and I_{ON}/I_{OFF} current ratio. Hence, the Cylindrical GAA MOSFET is one of the promising devices for nanoscale CMOS technology.

The purpose of this research is to analyze the Silicon Nanowire FET short channel effects on device performance based on different design parameters, and also to improve its reliability performance by optimizing the design parameters. The device used for this research study is Cylindrical Silicon Nanowire GAA TFET, by modelling the structure in Silvaco TCAD. This paper would measure the effect of different dielectric materials, the effect of different radius ranges, the effect of different oxide thickness, the effect of different gate metal work function and different drain voltage to study the various performance of electrical characteristics.

2. METHODOLOGY

2.1. Simulation and Modelling of Si-NW GAA TFET

The Silvaco TCAD suite is employed to model and simulate a Silicon Nanowire Gate-All-Around Tunneling Field-Effect Transistor (SiNW GAA TFET). Device fabrication is emulated using the Athena process simulator, while Atlas is used to analyze the device's electrical characteristics, including DC, AC, and transient responses, in both 2D and 3D simulation environments. DeckBuild serves as the primary simulation interface, and TonyPlot is utilized for the visualization and analysis of the output data. The study focuses on an n-type TFET (nTFET), which operates under positive gate and drain bias conditions. The device structure adopts a cylindrical GAA geometry, implemented via a tailored meshing scheme to ensure enhanced electrostatic control and improved current modulation relative to planar counterparts. This work used advanced physical models—including non-local band-to-band tunneling, Shockley–Read–Hall (SRH) recombination, and Auger recombination to accurately capture carrier transport and generation-recombination mechanisms. Material definitions and contact configurations are specified within Atlas prior to simulation, and the resulting electrical behavior is evaluated using TonyPlot. Critical geometrical and material parameters—such as gate oxide thickness (T_{OX}), channel radius, dielectric material, gate metal work function are systematically varied to assess their impact on device performance.

2.2. Flowchart

For the flow of the flowchart in Fig. 1 modelling of the silicon nanowire's material parameters need to be obtained and created to the material library of Silvaco tools. Right after adding the material, the software is ready to be used to design the device structure and study the features of the SiNW device. The modelling device used for simulation is Silicon Nanowire GAA TFET. The designed TFET, studied with various dimensions for channel radius (R), gate oxide thickness (T_{ox}) dielectric materials, gate metal work function and drain voltage to study the characteristics performance and analyze the importance of parameters effects on the device such as Subthreshold Slope (SS), threshold voltage (V_{TH}) and I_{ON}/I_{OFF} current ratio. All these design parameters are the input in the build deck of the Silvaco ATLAS tools.

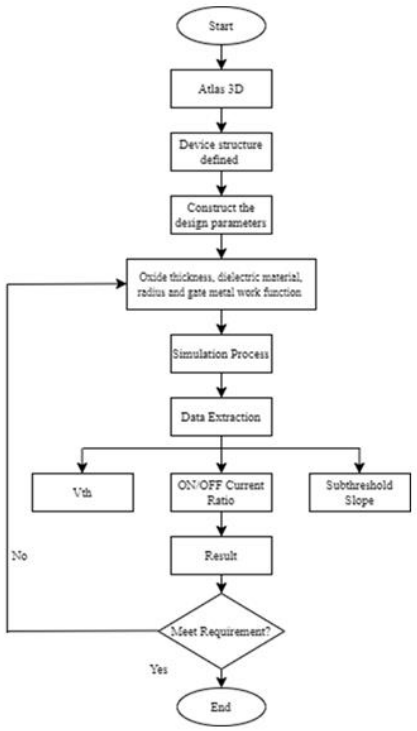

Figure 1. The flowchart of device modelling using Silvaco TCAD

2.3. Device Structure

The schematic diagram of Cylindrical GAA MOSFET that is used for modeling and simulation of this work is shown in Fig. 2. The source and drain of the device are uniformly doped with doping concentration of $N_D = 1 \times 10^{19}$ cm^{-3} with channel length of 25 nm and constant oxide thickness T_{OX} of 2 nm while the radius is 5 nm. HfO_2 has been used as a gate oxide dielectric where the metal gate work function simulated for the device is $\varphi_M = 4$ eV as stated in *Table II*.

This simulation demonstrates the capability of a TCAD simulation for Silicon Nanowire (NW) Gate-All-Around (GAA) Tunneling Field-Effect Transistor (TFET) which TFET is a gated p-i-n diode, where the source and drain are strongly doped with the gate controlling the band-to-band tunneling between the i-channel region and the p+ or n+ region by the bended energy band in the i-channel region [1] as in Fig. 4. The cross-section area of the device was pointed out at Fig. 3 where the structure was created by using Atlas Tools in Silvaco TCAD simulation. This is to study the electrical characteristics of Silicon NW-GAA-TFET at room temperature (300 K) with the constant drain voltages of 1.5 V [6].

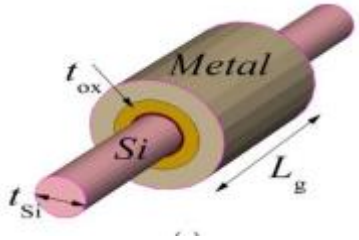

Figure 2. The schematic diagram of the Cylindrical Si NW GAA [2]

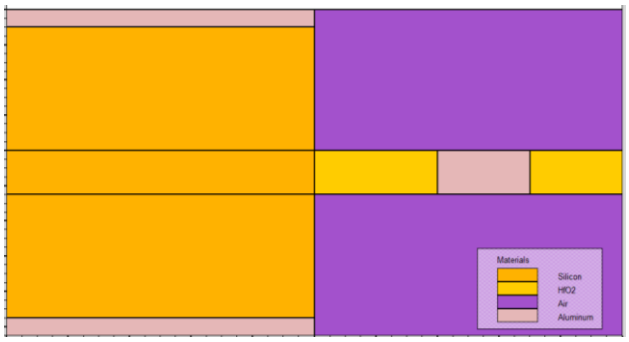

Figure 3. The cross-section structure of the SiNW GAA TFET

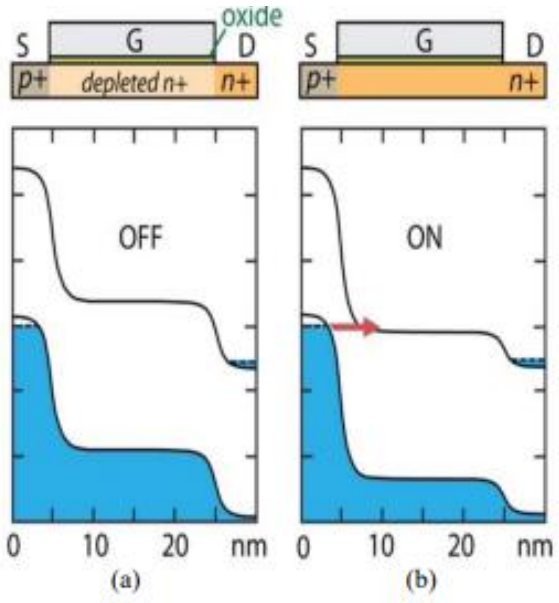

Figure 4. Energy band diagram and structure for TFET (a) Gate fully depletes the channel creating a normally off device. (b) The channel turns on with a positive gate voltage [7]

2.4. Design Parameters

A few parameters such as the radius of SiNW GAA TFET, oxide thickness, different gate metal work function, different channel length modulation of drain voltage and different types of dielectric material as stated in Table 1 would be discussed and investigated to understand the characteristics of SiNW GAA TFET device. For this simulation, the first step taken by channel radius has been varied, whereas other channel dimensions (ε_T, T_{ox} and φ_M) kept with constant values. For the second method, the effect of different dielectric material has been discussed with channel radius, gate metal work function and oxide thickness kept in constant values. For the next one, oxide thickness varied with channel radius, gate metal work function and dielectric material fixed. The last one parameter that varies is the gate metal work function. The variation of drain voltage (V_D) is also studied in this work. The value of constant parameter of channel radius, oxide thickness, dielectric material, drain voltage and gate metal work function is stated as in Table. 2.

Table 1. Design Parameters of SiNW Gaa TFET Model

Parameters	Values	Reference
Channel Radius (R)	5 nm,10 nm and 18 nm	[8]
Dielectric Material	SiO_2, HfO_2, Al_3O_2	[9], [10], [11]
Oxide Thickness (T_{OX})	2 nm,3 nm and 4 nm	[3] [8]
Gate Metal Work Function (φ_M)	TaN, TiN and Au	[12], [13]
Drain Voltage (V_D)	0.5 V, 1.5 V and 2.5 V	[6][14], [15]

Table 2. Constant Parameters Of SiNW GAA TFET Simulation

Parameters	Values
Channel Radius (R)	5 nm
Dielectric Material	HfO_2
Oxide Thickness (T_{OX})	2 nm
Channel Length (Lg)	25 nm
Source/Drain Doping	1×10^{19} cm^{-3}
Gate Metal Work Function	4
Drain and Source Length	80 nm
Gate Voltage (V_G)	0 to 1 V
Drain Voltage (V_D)	1.5 V
Nanowire Material	Silicon

2.5. Extraction of Electrical Characteristics

2.5.1. Subthreshold Slope (SS)

Subthreshold Slope measures how fast the drain current reacted by the gate voltage in the subthreshold region. The ideal value is 70 mV/decade at room temperature as stated in [16] which is mostly obtained in long channel devices. The subthreshold slope reciprocal value called subthreshold swing which is defined as:

$$S\,s\text{–}\,th = ln\,(10)\,\frac{kt}{q} + (1 + \frac{Cd}{Cox}) \quad (1)$$

2.5.2. I_{ON}/I_{OFF} Current Ratio

The measurement of current ratio would be measured at the I_D–V_G curve line. The I_{ON} would be the current that achieved at a logical "high" gate-voltage or at saturated current mode. It is the same with I_{OFF} where it would be the drain current with a logical low gate-voltage or at 0 V. Both of these curves were measured at a constant drain-source voltage.

2.5.3. Threshold Voltage, V_{TH}

The threshold voltage is one of the most promising MOSFET electrical characterization. It marks the turn-on point and separate the subthreshold area from the strong inversion area. The threshold voltage is also used to monitor the charge of oxides. Threshold voltage defined as the gate voltage obtained by extraction of the linear from the I_{ds}-V_{gs} curve from maximum slope to zero current drain [17]. The drain current of an ideal MOSFET in the linear area is stated by following:

$$I_D = \frac{\mu Cox W}{L} \left(V_{gs} - V_T - \frac{Vds}{2}\right) V_{ds} \quad (2)$$

Where μ is the carrier mobility, C_{ox} is the oxide capacitance, W is the channel width, L is the channel length, V_{gs} is the gate to source voltage, V_{ds} is the drain to source voltage, and V_T is the threshold voltage.

3. RESULT AND DISCUSSION

In this section, the impact of key design parameters—including oxide thickness, T_{OX}, nanowire radius, and gate dielectric material on the electrical performance of SiNW GAA TFETs is analyzed. The evaluation focuses on critical electrical characteristics such as threshold voltage, V_{TH}, subthreshold slope (SS), and the on/off current ratio, $I_{ON/OFF}$.

3.1. Effects of different oxide thickness

Oxide thickness is related to the oxide capacitance, as expressed in Equation 1

$$C_{OX} = \varepsilon_{ox} / T_{OX} \quad (3)$$

Where C_{ox} is oxide capacitance per unit area, ε_{ox} is the permittivity of gate dielectric, and T_{ox} is oxide thickness. Fig. 5 shows the variation of oxide thickness in relation to performance of electrical characterizations. Radius and dielectric material have been kept constant at 5 nm and HfO_2 respectively [8][10][18]. From the results in Fig. 5, it is clearly shown that at a lower size of oxide thickness, T_{ox}= 2 nm the TFET shows highest leakage current of SS characteristics, and improved SS value 78.3 mV/V is at T_{ox} = 4 nm. Improved SS while increasing the gate oxide thickness also proved in [8].

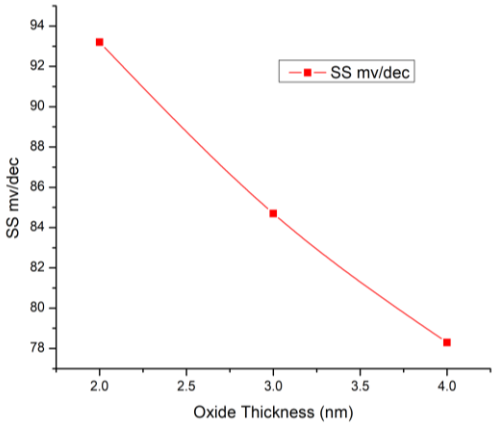

Figure 5. Subthreshold Slope with different oxide thickness

Fig. 6 shows both I_{ON} and I_{OFF} can be extracted from IV curve. The value of on current I_{ON} can be collected at Vgs = Vdd and subthreshold leakage I_{OFF} at Vgs = 0 V at saturation mode [15]. The minimum I_{ON}/I_{OFF} ratio with V_D = 1 V extracted at minimum T_{OX} = 2 nm which is ($0.01*10^3$) and then improved to ($0.10*10^3$) at T_{OX} = 4 nm. Fig. 6 also shows that the thinnest gate oxide thickness of 2 nm shows the minimum threshold voltage value while increasing the gate oxide thickness would increase the threshold voltage leading to better performance of the device.

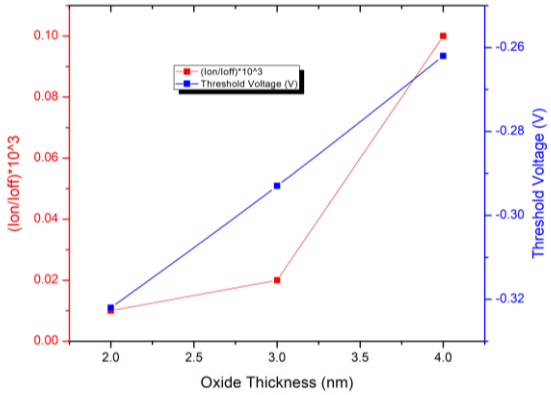

Figure 6. Current ratio and Threshold Voltage (Vth) with different oxide thickness

3.2. Effects of different radius

The effect of the channel radius on the electrical characteristics' performances has been discussed in this part. The values of radius (R) varied at 5 nm, 10 nm and 18 nm while constant parameters which are the T_{OX} and dielectric material measured at 5nm and HfO_2 respectively [8][10] [18].

Fig. 7 shows the performance of SS based on the changing channel radius (R). It shows the degradation of SS and high leakage current occurred at R = 5 nm which is 93.2 mV/dec while the SS highly improved at R=10 nm and R=18 nm which at 76.9 mV/dec and 75.9 mV/dec respectively where the SS approaches its ideal value of 70 mV/dec and also proved in [8].

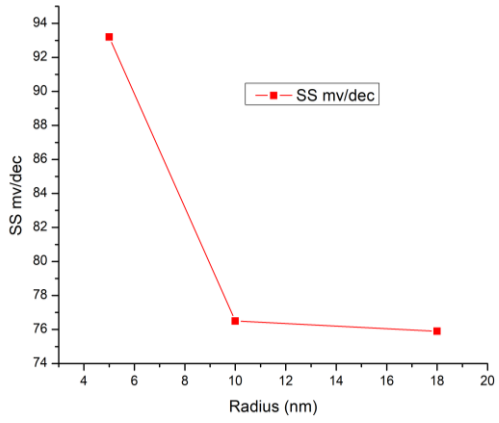

Figure 7. Subthreshold Slope with different radius

Fig. 8 depicts the electrical characteristics of I_{ON}/I_{OFF} ratio and V_{TH} based on the changing channel radius. These two electrical characteristics are proportionally increased with increasing channel radius. It stated that a channel radius higher than 10 nm would improvise the I_{ON}/I_{OFF} ratio where at R = 10 nm, the current ratio value is at $0.04*10^3$ meanwhile at R = 18 nm, the output of the current ratio gained its best value which is at $0.15*10^3$. However, at the lowest channel radius at 5 nm shows the decreasing of the I_{ON}/I_{OFF} ratio which is at $0.01*10^3$. Furthermore, the effect of

increasing the channel radius also shown the changes on the threshold voltage (Vth) where the Vth dropped to -0.32V at R = 5 nm. The value is slightly improved at R = 10 nm where the voltage at -0.29 V. The highest channel radius, which is 18 nm rapidly increases the value at V_{TH} = -0.11V.

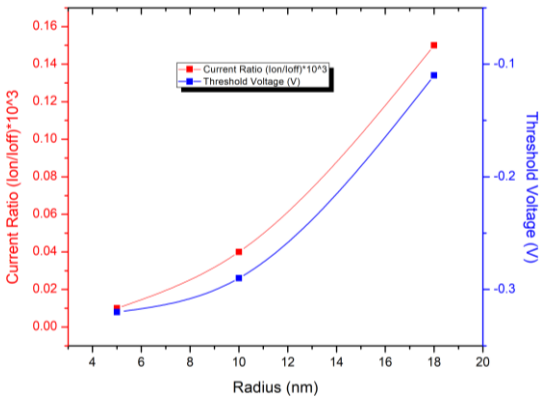

Figure 8. Current ratio and threshold voltage (Vth) with different radius

3.3. Effects of different dielectric material

From the electrical characteristics, the variations of SS, I_{ON}/I_{OFF} ratio and V_{TH} are plotted in Fig. 9 and Fig. 10. As for the simulation of the different dielectric materials, the various dielectric materials are SiO_2, Al_2O_3 and HfO_2. Fig. 9 shows the decreasing of SS value with the use higher gate dielectrics in SiNW GAA TFET. The plot shows that the SiO_2 and Al_2O_3 have lower SS as compared to HfO_2 implying that HfO_2 has inferior SS characteristics than those two dielectrics. With SiO_2 SS value at 57.3 mV/dec, it almost obtains an ideal value of 70 mV/dec.

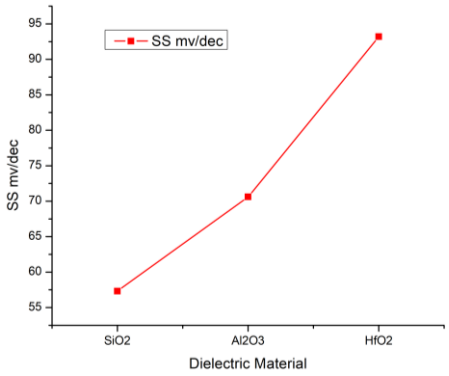

Figure 9. Subthreshold Slope with different dielectric material

The current ratio I_{ON}/I_{OFF} with different dielectric materials is plotted in Fig. 10. The plot shows that I_{ON}/I_{OFF} ratio improves with the relative dielectric of gate oxide in SiNW GAA TFET which indicates that SiO_2 to be better than Al_2O_3 and HfO_2 as dielectric. This is due to SiO_2 having far lower I_{OFF} current than Al_2O_3 and HfO_3 even SiO_2 has slightly lower I_{ON} current than those two dielectrics. Meanwhile for the threshold voltage V_{th}, it also shows that SiO_2 is better in terms of Vth rather than Al_2O_3 and HfO_2 where it against the studies in [19] as HfO_2 is better in terms of characteristics performance.

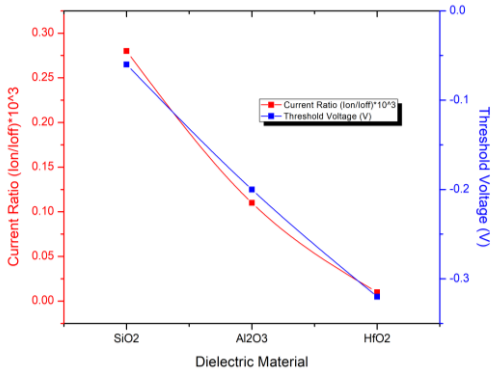

Figure. 10. Current ratio and threshold voltage (Vth) with different dielectric materials

3.4. Effects of different gate metal work function

In this section, SiNW GAA TFET is simulated with three different gate metal work functions which are 4 eV, 4.4 eV and 4.8 eV for TaN, TiN and Au respectively. The electrical characteristics of different gate metal work functions are shown in Fig. 11 and Fig. 12.

Figure 11 shows the result of the variation in Subthreshold Slope (SS) where it indicates that as work function of gate metal increase, the value of SS would be better in its values. It shows that 4.4 eV TiN and 4.8 eV Au obtain slightly better than ideal value of 70 mV/dec.

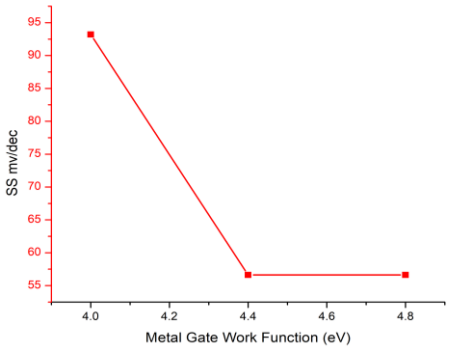

Figure. 11. Subthreshold Slope with different gate metal work function

Fig. 12 shows the variation in I_{ON}/I_{OFF} current ratio and threshold voltage V_{TH}. From the result, it concludes that the 4.8 eV Au has the least current ratio while 4.4 eV TiN performance on current ratio is the best one and slightly better than 4.4 eV TaN. Meanwhile, as the work function of metal gate increases, it shows an increase in the values of threshold voltage, V_{TH}. The result in the three characteristics performance shows that work function of 4.4 eV TiN is the most ideal and stable gate metal as proved in studies [20] where the better work function is 4.5 eV as it has the ideal SS, and acceptable values of current ratio and threshold voltage.

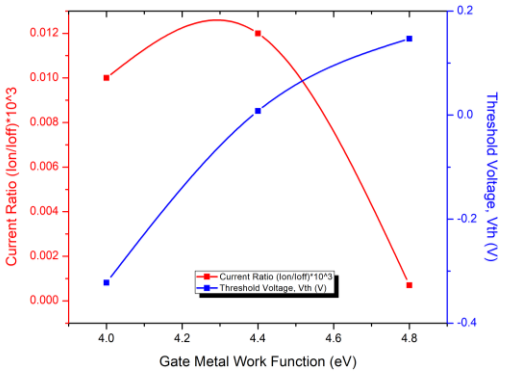

Figure. 12. Current ratio and Threshold Voltage (Vth) with gate metal work function

3.5. Effects Of Different Drain Voltage

The effect different drain voltage has been simulated for the studied device where variation of drain voltage is at 0.5 V, 1.5 V and 2.5 V. Fig. 13 shows the performance of SS based on the changing the drain voltage. It shows that the degradation of SS at 0.5 V and 1.5 V where the two-drain voltage is almost the same when it comes to its subthreshold slope values. While the increasing drain voltage at 2.5 V resulting in a better performance of the subthreshold slope where it almost reached the 50 mV/dec resulting in low leakage current, however it decreases in performance as in Fig. 14 where studies in [15] shows that increasing supply voltage would lead the device suffering in high SCEs.

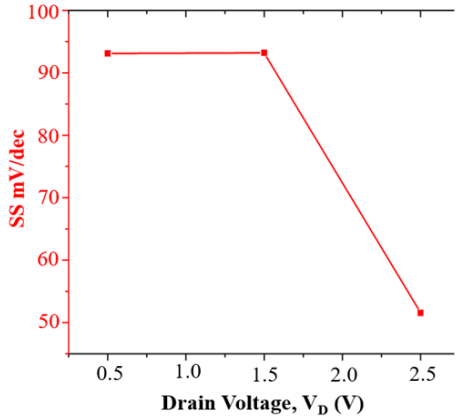

Fig. 13. Subthreshold Slope with different drain voltage (V_D)

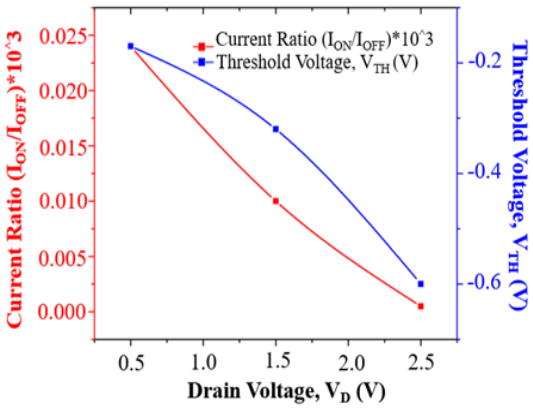

Fig. 14. Current ratio and Threshold Voltage (V_{TH}) with different drain voltage (V_D)

The next result shown in Fig. 14 is the variation of I_{ON}/I_{OFF} and V_{TH} affected in three different values of drain voltage where the characteristics performance indicates the similar respond. When the drain voltage increases, the value of the current ratio and V_{TH} decreases. The results indicate that 0.5 V of drain voltage has the most stable performance for this device as it has the ability to stabilize the SCEs as in [15].

4. CONCLUSION

Various simulation results for SiNW GAA TFET structure have been presented in this research paper. From the research study, changes of the oxide thickness, channel radius, dielectric material, gate metal work function and drain voltage deeply affecting the performance of the device, in terms of performance variation on parameters such as subthreshold slope (SS), I_{ON}/I_{OFF} current ratio and threshold voltage (V_{TH}). The result shows that the oxide thickness with better parameters characteristics is at 4 nm where it reached reasonable value of SS, I_{ON}/I_{OFF} current ratio and threshold voltage (V_{TH}). For the channel radius, the range with good characteristics performance is up to 10 nm -18 nm whereas the changing of dielectric material of SiO_2, Al_2O_3 and HfO_2 shows that the SiO_2 dielectric comes up with the best characteristics for this device modelling. The work function of 4.4 eV TiN is the most suitable gate metal with its stability in characterization of the simulation while the effective value of drain voltage for the SiNW GAA TFET is at 0.5 V.

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