Geometry-Dependent Carrier Mobility in Nanosheet FETs and Its Impact on Logic Circuit Performance

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ABSTRACT

This work investigates the effects of geometric and material parameter variations of Gate-All-Around Nanosheet FET (NsFET) on both the device and circuit levels. As device scaling approaches the 5nm domain, conventional technologies like FinFET face significant design challenges due to short channel effects such as leakage current and reduced drain potential barriers. NsFET has a gate-all-around design that provides a promising solution by offering stronger electrostatic control that mitigates short channel effects during downscaling. In this work, the BSIM CMG model was used with the Synopsys HSPICE Simulator to analyse the influence of geometric parameter variations on the NsFET device performance. At the device level, the 𝐼𝑜𝑛/𝐼𝑜𝑓𝑓 ratio shows the greatest sensitivity to temperature and nanosheet thickness variations with the lowest off-state current observed at -45°C (𝐼𝑜𝑓𝑓 = 1.03 𝑓𝐴) and 𝑇𝑁𝑆 = 4𝑛𝑚 (𝐼𝑜𝑓𝑓 = 43.72 𝑓𝐴). The inverter circuit analysis reveals the shortest propagation delay, 𝑇𝑝 = 33.75 𝑝𝑠, with dynamic power of 3.35 𝜇𝑊 and static power of 10.7 𝑛𝑊 at 𝑉𝐷𝐷 = 1.2𝑉. Higher supply voltages enhance switching speed, resulting in higher dynamic and static power consumption. It was observed that the nanosheet number variations had the most significant impact on propagation delay. The inverter circuit uses a Pseudo Random Binary Signal (PRBS) to more closely imitate real-world input conditions. In the 5-stage ring oscillator circuit, the frequency of oscillation is most influenced by gate length (𝐿𝐺) variation, achieving 𝑓𝑜𝑠𝑐 = 2.965 𝐺𝐻𝑧 at 𝐿𝐺 = 6𝑛𝑚. The 𝑓𝑜𝑠𝑐 decreases as load capacitance increases with additional stages from 5 to 7 then to 9 stages. The research later shifts focus to optimizing NsFET based 6T SRAM cell by developing a weightage table for performance parameters, including write/read power, stability margins, and timing, while exploring the effects of transistor sizing, number of nanosheets, supply voltage, and temperature. The optimized NsFET 6T SRAM cell of parameters, 𝐶𝑅 = 1, 𝑃𝑅 = 0.5, 𝐿𝐺 = 14𝑛𝑚, 𝑛𝑁𝑆𝑎𝑐𝑐𝑒𝑠𝑠 = 2, 𝑛𝑁𝑆𝑙𝑎𝑡𝑐ℎ = 1, 𝑉𝐷𝐷 = 0.7𝑉 showed an overall improvement of 14.36% with greater read, write and hold static noise margins. This study aids in enhancing NsFET fabrication methods and improving circuit design approaches, ensuring that their capabilities are effectively harnessed in real-world applications.

Keywords: Gate-All-Around Nanosheet FET (NsFET), electrostatic, geometric, temperature and nanosheet thickness