Electrical Performance Evaluation Based on Design Parameters of Silicon Nanowire Gate-All-Around (GAA) TFET

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ABSTRACT

The Silicon Nanowire Gate-All-Around (SiNW GAA) is one of the technologies with potential for improved short-channel behavior and gate control over conductivity. This work investigates the effect of various geometrical dimensions on the electrical characteristics of SiNW GAA Tunneling Field-Effect Transistor (TFET). The design parameters, including gate oxide thickness (TOX), channel radius, dielectric material, gate metal work function, and low or high drain voltage, are varied in the simulation process to analyze the electrical performance of SiNW GAA TFET. Subthreshold Slope (SS), ION/IOFF current ratio, and threshold voltage (Vth) are extracted. The results demonstrate that an oxide thickness of 3 nm, a channel radius of 10 nm to 18 nm, and SiO2 as a dielectric material tend to yield the best SiNW GAA TFET characteristics. In contrast, the work function of the gate metal TiN and a drain voltage of 0.5 V are the most effective for device performance. This study highlights the potential of GAA nanowire TFETs to drive innovation in semiconductor technology through superior electrical performance.

**Keywords:** SiNW GAA TFET; gate oxide thickness TOX; channel radius; dielectric material; gate metal work function; drain voltage; Subthreshold Slope (SS); ION/IOFF current ratio; Threshold Voltage (Vth)

# INTRODUCTION

The scaling of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) has continued since the development of integrated circuits in the 1950s, with the emergence of new technologies extending Complementary Metal-Oxide-Semiconductor (CMOS) technology to increasingly smaller technological nodes. However, due to basic physical and technical restrictions, CMOS scaling has deviated from Moore’s predicted trends and Dennard scaling’s principles [1]. Moore’s Law states that every 24 months, the number of transistors on a chip doubles [2]. The scaling faces several challenges, including leakage current, static power dissipation, performance limitations due to the Subthreshold Slope (SS), threshold voltage (Vth) issues, and other related Short-Channel Effects (SCE) [3], [4].

Heat dissipation, leakage current, and channel length modulation have all become significant concerns, which will eventually slow down CMOS scaling as the technology approaches the atomic dimension [5], [6]. As a result, new semiconductor technologies are urgently needed to address challenges such as cost, speed, reliability, and power dissipation. A significant amount of effort has been invested by all the candidates, and Nano-Electronics, involving the replacement of existing silicon-based technology, has emerged as one of the most promising solutions for continuous CMOS scaling [7] .

In recent decades, bottom-up semiconductor nanowires and their derived Field-Effect Transistors (FET) have been extensively explored as essential building blocks for nano electronic devices and circuit technologies. Nanowires have a smaller channel and a higher surface-to-volume ratio than planar devices made of bulk materials. Furthermore, the gate surrounding or Gate All Around (GAA) structure that may be produced in nanowire FETs provides good electrostatic gate control over the nanowire channel. This GAA-based FET technology exhibits excellent resistance to SCE, high packing density, enhanced drain current drivability, and superior overall performance [8].

Silicon Nanowire (SiNW) FET were listed as one of the most promising emerging logic devices and are ideal for ultra-low-power logic circuit integration. However, the configuration has limited reliability, and detailed research is needed to address the reliability and performance concerns of these Si-based MOSFETs [9]. In addition to their limitations in fabrication and scaling for threshold voltages, gate oxide thicknesses, and leakage currents, the occurrence of SCEs, such as Subthreshold Slope (SS) and gate current leakage in the transistor, complicates the scaling process.

On the other hand, further study is required to overcome these problems, and the Cylindrical GAA MOSFET is considered a promising device for CMOS technology. Studies in [10] indicate that the GAA FET exhibits superior performance compared to other devices in terms of scaling of SCEs such as SS, threshold voltages (Vth), and ION/IOFF current ratio. Hence, the Cylindrical GAA MOSFET is one of the promising devices for nanoscale CMOS technology.

The purpose of this research is to analyze the SiNW FET SCE’s device performance based on different design parameters and to improve its reliability by optimizing these parameters. The device used in this research study is a Cylindrical SiNW GAA TFET, modeled in Silvaco Technology Computer-Aided Design (TCAD). Additionally, this paper aims to measure the effects of different dielectric materials, various radius ranges, different oxide thicknesses, different gate metal work functions, and different drain voltages on the performance of electrical characteristics.

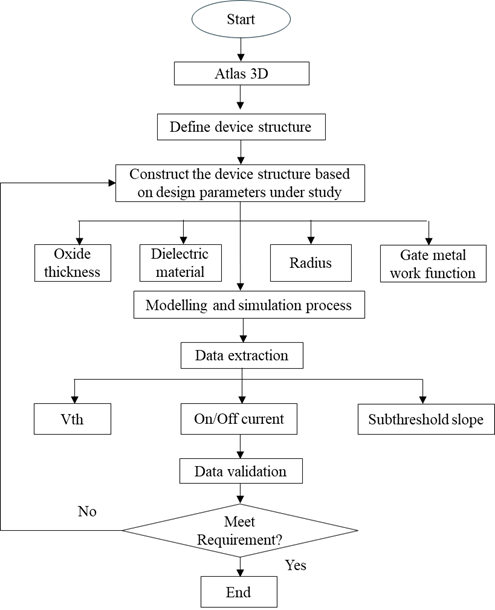
# METHODOLOGY

## Simulation and Modelling of Si-NW GAA TFET

The Silvaco TCAD suite is employed to model and simulate a Silicon Nanowire Gate-All-Around Tunneling Field-Effect Transistor (SiNW GAA TFET). Device fabrication is emulated using the Athena process simulator, while Atlas is used to analyze the device’s electrical characteristics, including DC, AC, and transient responses, in both 2D and 3D simulation environments. DeckBuild serves as the primary simulation interface, and TonyPlot is utilized for the visualization and analysis of the output data. The study focuses on an n-type TFET (nTFET), which operates under positive gate and drain bias conditions. The device structure employs a cylindrical GAA geometry, implemented through a tailored meshing scheme to ensure enhanced electrostatic control and improved current modulation relative to planar counterparts. This work employed advanced physical models, including non-local band-to-band tunneling, Shockley–Read–Hall (SRH) recombination, and Auger recombination to accurately capture carrier transport and generation-recombination mechanisms. Material definitions and contact configurations are specified within Atlas prior to simulation, and the resulting electrical behavior is evaluated using TonyPlot. Critical geometrical and material parameters—such as gate oxide thickness (TOX), channel radius, dielectric material, and gate metal work function are systematically varied to assess their impact on device performance.

## Flowchart

To model the flowchart in Fig. 1, the material parameters of the SiNW must be obtained and added to Silvaco’s material library. Immediately after adding the material, the software is ready for use in designing the device structure and studying the features of the SiNW device. The modelling device used for simulation is SiNW GAA TFET. The designed TFET was studied with various dimensions for channel radius (R), gate oxide thickness (Tox), dielectric materials, gate metal work function, and drain voltage. These variations were used to evaluate the device’s characteristics and analyze the effects of parameters, such as SS, threshold voltage (VTH), and ION/IOFF current ratio. All these design parameters are inputs to the build deck of the Silvaco ATLAS tools.



**Figure 1**. The flowchart of Si-NW GAA TFET modelling using Silvaco TCAD

## Device Structure and Design Parameter Details

The schematic diagram of the Cylindrical GAA MOSFET used for modeling and simulation in this work is illustrated in Fig. 2, with the cross-sectional area of the device highlighted in Fig. 3, where the structure was created using Atlas Tools in Silvaco TCAD simulation. This simulation demonstrates the capability of TCAD for SiNW GAA TFET. The TFET operates as a gated p-i-n diode, with the heavily doped source and drain regions. The gate controlling the band-to-band tunneling between the i-channel region and the p+ or n+ region by bending the energy band in the i-channel region [1] as in Fig. 4. This analysis aims to investigate the electrical characteristics of SiNW-GAA-TFET at room temperature (300 K) with the constant drain voltages of 1.5 V [11].

A diagram of a channel

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**Figure 2**. The schematic diagram of the Cylindrical SiNW GAA demonstrating the source, drain, gate, and channel [2]

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**Figure 3**. The cross-section structure of the SiNW GAA TFET shows the gate, dielectric and substrate

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**Figure 4**. Energy band diagram and structure for TFET (a) Zener tunneling p+ n+ channel (b) Gate fully depletes the channel, creating a normally off device. (c) The channel turns on with a positive gate voltage [12]

In this work, the design parameters, including channel radius, dielectric material, oxide thickness, gate metal work function, and drain voltages, were varied to characterize and evaluate the device’s performance comprehensively. Specifically, the design parameters are varied based on the details stated in Table 1. Table 2 presents the fixed parameter values when the respective design parameters are varied accordingly. These include the source and drain of the device being uniformly doped with a doping concentration of ND = 1 × 1019 cm-3 with a channel length of 25 nm and a constant oxide thickness TOX of 2 nm, while the radius is 5 nm. Moreover, HfO2 has been used as a gate oxide dielectric, and the metal gate work function simulated for the device is φM = 4 eV.

**Table 1.** Design Parameters of SiNW GAA TFET Model

|  |  |  |
| --- | --- | --- |
| **Parameters** | **Values** | **Reference** |
| Channel Radius (R) | 5 nm,10 nm, and 18 nm | [13] |
| Dielectric Material | SiO2, HfO2, Al3O2 | [14], [15], [16] |
| Oxide Thickness (TOX) | 2 nm,3 nm, and 4 nm | [3] [13] |
| Gate Metal Work Function (φM) | TaN, TiN, and Au | [17], [18] |
| Drain Voltage (VD) | 0.5 V, 1.5 V, and 2.5 V | [11][19], [20] |

**Table 2.** Constant Parameters Of SiNW GAA TFET Simulation

|  |  |
| --- | --- |
| **Parameters** | **Values** |
| Channel Radius (R) | 5 nm |
| Dielectric Material | HfO2 |
| Oxide Thickness (TOX) | 2 nm |
| Channel Length (Lg) | 25 nm |
| Source/Drain Doping | 1 × 1019 cm-3 |
| Gate Metal Work Function | 4 |
| Drain and Source Length | 80 nm |
| Gate Voltage (VG) | 0 to 1 V |
| Drain Voltage (VD) | 1.5 V |
| Nanowire Material | Silicon |

## Extraction of Electrical Characteristics

### Subthreshold Slope (SS)

Subthreshold Slope (SS) measures the rate at which the drain current responds to the gate voltage in the subthreshold region. The ideal value is 70 mV/dec at room temperature, as stated in [21] which is typically obtained in long-channel devices. The SS reciprocal value, called subthreshold swing, is defined as:

|  |
| --- |
| *S s– th = ln (10)*  *+ (1 + ).*  (1) |

### ION/IOFF Current Ratio

The measurement of the current ratio would be made at the ID–VG curve line. The ION would be the current achieved at a logical “high” gate-voltage or saturated current mode. The same applies to IOFF, where it represents the drain current with a logical low gate voltage or at 0 V. Both of these curves were measured at a constant drain-source voltage.

### Threshold Voltage, VTH

The threshold voltage is one of the most important electrical characteristics of MOSFET. It marks the turn-on point and separates the subthreshold area from the strong inversion area. Additionally, the threshold voltage is also used to monitor the charge of oxides. By definition, threshold voltage is the gate voltage obtained by extracting the linear region from the Ids-Vgs curve from the maximum slope to zero current drain [22]. The drain current of an ideal MOSFET in the linear area is stated by the following:

|  |
| --- |
| *ID = (Vgs – VT - ) Vds,*  (2) |

where *µ* is the carrier mobility, *Cox* is the oxide capacitance, W is the channel width, *L* is the channel length, Vgs is the gate to source voltage, Vds is the drain to source voltage, and VT is the threshold voltage.

# RESULT AND DISCUSSION

In this section, the impact of key design parameters—such as oxide thickness, TOX, nanowire radius, and gate dielectric material on the electrical performance of SiNW GAA TFETs is analyzed. The evaluation focuses on critical electrical characteristics such as threshold voltage, VTH, SS, and the on/off current ratio, ION/OFF.

## Effects of different oxide thickness

Oxide thickness is related to the oxide capacitance, as expressed in Equation 3:

|  |
| --- |
| COX = εox / TOX,(3) |

where Cox is oxide capacitance per unit area, εox is the permittivity of the gate dielectric, and Tox is oxide thickness. Fig. 5 illustrates the variation of oxide thickness in relation to the performance of electrical characterizations. The radius and dielectric material have been kept constant at 5 nm and HfO2, respectively [13][15][23]. From the results in Figure 5, it is demonstrated that at a lower oxide thickness, Tox = 2 nm, the TFET exhibits the highest leakage current and SS characteristics, with an improved SS value of 78.3 mV/V at Tox = 4 nm. Improving the SS while increasing the gate oxide thickness has also been proven in [13].

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**Figure 5**. Subthreshold slope with different oxide thickness 2 nm, 3 nm and 4 nm

Fig. 6 illustrates that both ION and IOFF can be extracted from the ID–VG curve line. The value of the current ION can be collected at Vgs = Vdd, and the subthreshold leakage IOFF is observed at Vgs = 0 V in saturation mode [19]. The minimum ION/IOFF ratio, with VD = 1 V, was extracted at a minimum TOX = 2 nm, which is (0.01\*103), and then improved to (0.10\*103) at TOX = 4 nm. Figure 6 also demonstrates that the thinnest gate oxide thickness of 2 nm yields the minimum threshold voltage value, while increasing the gate oxide thickness increases the threshold voltage, resulting in improved device performance.

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**Figure 6.** Current ratio and threshold voltage with different oxide thickness, 2 nm, 3 nm and 4 nm

## Effects of different radius

The effect of the channel radius on the electrical characteristics’ performance has been discussed in this section. The values of radius (R) varied at 5 nm, 10 nm, and 18 nm, while the constant parameters, TOX and dielectric, were measured at 5nm and HfO2, respectively [12][14][22].

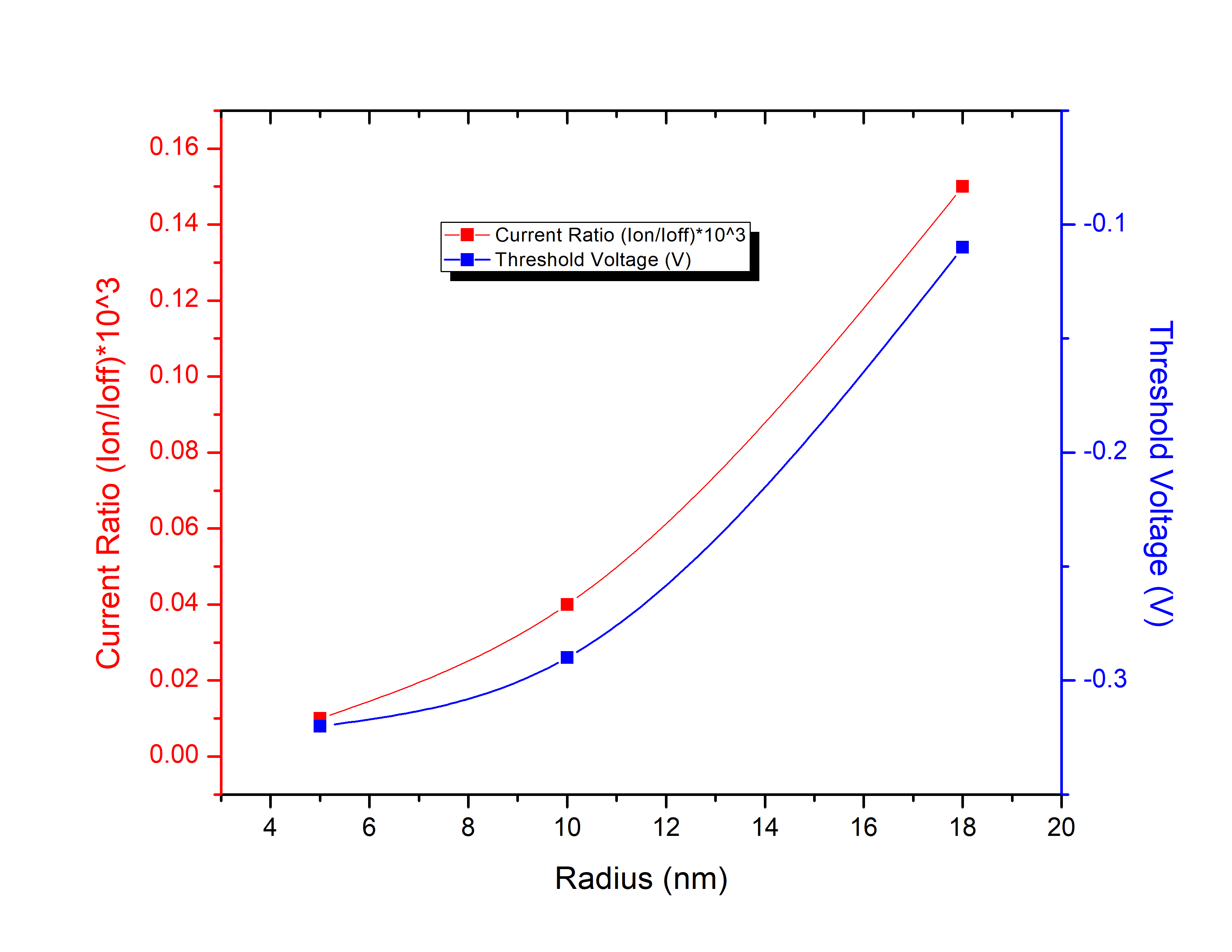
Fig. 7 illustrates the performance of the SS as a function of the changing channel radius (R). It demonstrates the degradation of SS and high leakage current, which occurred at R = 5 nm, with a slope of 93.2 mV/dec. In comparison, the SS demonstrated significant improvement at R = 10 nm and R = 18 nm, with slopes of 76.9 mV/dec and 75.9 mV/dec, respectively. These values indicate that the SS approaches its ideal value of 70 mV/dec, as also demonstrated in [12].

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**Figure 7.** Subthreshold slope with different radius, 5 nm, 10 nm, 18 nm

Fig. 8 depicts the electrical characteristics of the ION/IOFF ratio and threshold voltage based on the changing channel radius. These two electrical characteristics are proportionally increased with increasing channel radius. It stated that a channel radius higher than 10 nm would improve the ION/IOFF ratio, where at R = 10 nm, the current ratio value is 0.04\*103. At R = 18 nm, the output current ratio reached its optimal value of 0.15\*103. However, at the lowest channel radius of 5 nm, the ION/IOFF ratio decreases to 0.01\*103. Furthermore, the effect of increasing the channel radius is also demonstrated, with changes in the threshold voltage, where the threshold voltage dropped to -0.32 V at R = 5 nm. The value is slightly improved at R = 10 nm, where the voltage is -0.29 V. The highest channel radius, which is 18 nm, rapidly increases the value at a threshold voltage of -0.11 V.



**Figure** 8. Current ratio and threshold voltage with different radius, 5 nm, 10 nm, 18 nm

## Effects of different dielectric materials

From the electrical characteristics, the variations of SS, ION/IOFF ratio, and threshold voltage are plotted in Fig. 9 and 10. As for the simulation of the different dielectric materials, the various dielectric materials are SiO2, Al2O3, and HfO2. Furthermore, Fig. 9 illustrates the increase in SS value with the use of higher gate dielectrics in SiNW GAA TFET. The plot demonstrates that SiO2 and Al2O3 have lower SS compared to HfO2, implying that HfO2 has inferior SS characteristics compared to these two dielectrics. With a SiO2 SS value of 57.3 mV/dec, it almost achieves the ideal value of 70 mV/dec.

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**Figure** 9. Subthreshold slope with different dielectric materials, SiO2, AlO2O3 and HfO2

The current ratio ION/IOFF with different dielectric materials is plotted in Fig. 10. The plot demonstrates that the ION/IOFF ratio improves with the relative dielectric constant of the gate oxide in SiNW GAA TFET, indicating that SiO2 is better than Al2O3 and HfO2 as a dielectric. This is due to SiO2 exhibiting significantly lower IOFF current compared to Al2O3 and HfO2, despite having a slightly lower ION current than both dielectrics. On the other hand, for the threshold voltage, it also demonstrates that SiO2 is superior to Al2O3 and HfO2, which aligns with the studies in [23], as HfO2 exhibits better characteristic performance. Higher k-values are typically associated with a greater density of interfacial trap charges, which can contribute to performance reduction in high-k dielectric devices [24].

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**Figure**. 10. Current ratio and threshold voltage with different dielectric materials, SiO2, AlO2O3 and HfO2

## Effects of different gate metal work functions

In this section, SiNW GAA TFET is simulated with three different gate metal work functions: 4 eV, 4.4 eV, and 4.8 eV for TaN, TiN, and Au, respectively. The electrical characteristics of different gate metal work functions are illustrated in Fig. 11 and Fig. 12.

Fig. 11 illustrates the result of the variation in SS, indicating that as the work function of the gate metal increases, the value of the SS improves. It demonstrates that 4.4 eV TiN and 4.8 eV Au obtain slightly better than the ideal value of 70 mV/dec.

A graph of metal gate work function

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**Figure**. 11. Subthreshold slope with different gate metal work function, 4eV, 4.4eV and 4.8eV

Fig. 12 presents the variation in the ION/IOFF current ratio and threshold voltage. From the results, it is concluded that the 4.8 eV Au has the least current ratio, while the 4.4 eV TiN has the best performance in terms of current ratio, being slightly better than the 4.4 eV TaN. Consequently, as the work function of the metal gate increases, the threshold voltage values also increase. The results in the three characteristics of performance exhibit that the work function of 4.4 eV TiN is the most ideal and stable gate metal, as proven in studies [25]. The optimal work function is 4.5 eV, as it has the ideal SS, and acceptable values of current ratio and threshold voltage. Additionally, TiN is an ideal metal gate material for advanced MOSFETs due to its wide work function tunability (4.52–4.03 eV), along with excellent thermal and chemical stability, making it highly suitable for low-power, low-voltage operation [26].

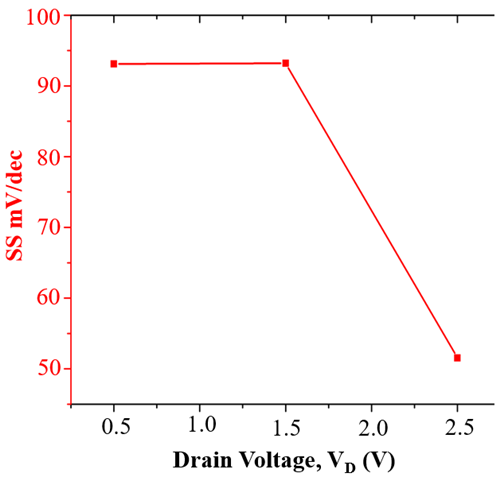
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**Figure**. 12. Current ratio and threshold voltage with gate metal work function, 4eV, 4.4eV and 4.8eV

## Effects Of Different Drain Voltages

The effect of different drain voltages has been simulated for the studied device, with drain voltage variations of 0.5 V, 1.5 V, and 2.5 V. Fig. 13 illustrates the performance of the SS based on the change in drain voltage. It demonstrates that the degradation of SS occurs at 0.5 V and 1.5 V, where the two-drain voltage values are almost the same in terms of their SS. In contrast, the increasing drain voltage at 2.5 V results in improved performance of the SS, where it nearly reaches the 50 mV/dec, resulting in a low leakage current. However, it decreases in performance, as illustrated in Fig. 14, where studies in [20] demonstrate that increasing the supply voltage would lead the device to suffer from high SCEs.



**Figure**. 13. Subthreshold slope with different drain voltage, 0.5 V, 1.5 V and 2.5 V (VD)

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**Figure.** 14. Current ratio and threshold voltage with different drain voltage (VD), 0.5 V, 1.5 V and 2.5 V

Fig. 14 presents the subsequent results, demonstrating the variation of ION/IOFF and threshold voltageacross three different values of drain voltage, where the characteristics’ performance indicates a similar response. When the drain voltage increases, the value of the current ratio and threshold voltagedecreases. Hence, the results indicate that a drain voltage of 0.5 V yields the most stable performance for this device, as it can stabilize the SCEs as reported in [19].

# conclusion

Various simulation results for the SiNW GAA TFET structure are presented in this research paper. According to the study, changes in oxide thickness, channel radius, dielectric material, gate metal work function, and drain voltage have a significant impact on the device’s performance, affecting parameters such as SS, ION/IOFF current ratio, and threshold voltage. The result reveals that the oxide thickness with better parameter characteristics is 4 nm, achieving a reasonable value of SS, ION/IOFF current ratio, and threshold voltage. For the channel radius, the range with good characteristic performance is 10 nm to 18 nm. Additionally, the change in dielectric material from SiO2 to Al2O3 and HfO2 demonstrates that the SiO2 dielectric yields the best characteristics for this device modelling. Notably, the work function of 4.4 eV TiN is the most suitable gate metal with its stability in characterization of the simulation, while the effective value of drain voltage for the SiNW GAA TFET is at 0.5 V. These findings provide a foundation for future experimental validation through fabrication and characterization of SiNW GAA TFET prototypes, which would help verify the simulation outcomes and assess their applicability under real-world conditions.

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